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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/828,556	04/21/2004	Takashi Noma	492322017700	5433

25227 7590 05/25/2005

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EXAMINER	
PAREKH, NITIN	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 05/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/828,556	NOMA ET AL.	
	Examiner	Art Unit	
	Nitin Parekh	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 April 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) *9-15* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 April 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12-17-04,04-21-04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restriction

1. Applicant's election without traverse of Group I, claims 1-8 in Paper No. 2 is acknowledged.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

3. Claims 1-8 are rejected under 35 U.S.C. 102(a) as being anticipated by Yamada et al. (see IDS reference: Yamada et al., US Pat. App. Pub. No. 2002/0047210).

Regarding claim 1, Yamada et al. disclose a semiconductor device comprising:

- a semiconductor chip/substrate (see top/middle chip 202 in Fig. 42)
- a first electrode/wiring formed under an insulation film (see 209 and 208 respectively in Fig. 42) formed on a front surface of the semiconductor chip
- a second electrode/wiring (205 in Fig. 42) formed on the insulation film
- a supporting insulating layer/body bonded to the front surface (see 210 in Fig. 42) and having an opening to expose at least part of the second wiring, and

- a third wiring (206/207 in Fig. 42) disposed on an insulation/additional insulation film (see 208 on the surface 203/204 in Fig. 42) formed on a back surface of the semiconductor chip, extending along a side surface of the semiconductor chip, and connected to the first wiring

(Fig. 42; section 0326; pp. 2-25).

Yamada et al. further disclose the first electrode/wiring being conventionally formed on an insulation film (see 112 and 115 respectively in Fig. 39) on the front surface of the chip (section 0303).

Regarding claims 2-4, Yamada et al. disclose the entire claimed structure as applied to claim 1 above, wherein Yamada et al. further disclose a connection member/conductive terminal (see 211 in Fig. 42; section 0326) comprising a projecting electrode terminal in a form of a metal ball/solder bump (see 306 in Fig. 52; section 0375) being disposed on the third wiring.

Regarding claims 5-8, Yamada et al. disclose the entire claimed structure as applied to claims 1-4 above, wherein Yamada et al. further disclose a stacked device having a second semiconductor chip/device being disposed on the first semiconductor device such that the conductive terminal on the back surface of the second semiconductor chip is connected to the second electrode/wiring of the first semiconductor device through the opening of the supporting insulating layer/body (see the stacked structure in Fig. 42

having a plurality of chips 202 including top two chips, each chip having respective electrode/wiring, terminals and insulating/supporting films).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Parekh whose telephone number is 571-272-1663. The examiner can normally be reached on 09:00AM-05:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9318.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Nitin Parekh

NP

05-23-05

NITIN PAREKH

PRIMARY EXAMINER

TECHNOLOGY CENTER 2800